## Remarks

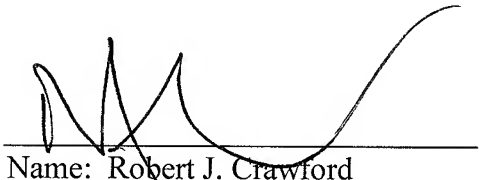
The non-final Office Action dated April 10, 2008 listed the following rejections: claims 1-2, 8-9, 11-12, 14-17, 19-20 and 25-26 stand rejected under 35 U.S.C. § 102(e) over Launiainen (U.S. 7,114,089); and claim 10 stands rejected under 35 U.S.C. § 103(a) over Launiainen in view of the Official Notice as exemplified by Dinechin (U.S. 2003/0177482). The Office Action also indicated that claims 27-30 are allowed and that claims 3-7, 13 and 21-24 would be allowable if rewritten in independent form. In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 102(e) rejection of claims 1-2, 8-9, 11-12, 14-17, 19-20 and 25-26 and the § 103(a) rejection of claim 10 because the claimed invention was conceived of prior to the reference date of Launiainen (*i.e.,* the U.S. filing date of Oct. 4, 2002), as evidenced by the 37 C.F.R. § 1.131 Declarations submitted herewith, showing correspondence between the claimed invention and a document entitled "power_down operation: a method to reduce power dissipation of microprocessors" (label Exhibit A), dated before Oct. 4, 2002 (date having been redacted pursuant to M.P.E.P. § 715.07(II)). According to M.P.E.P. § 2136, "The prior art date of a reference under 35 U.S.C. 102(e) may be the international filing date if the international filing date was on or after November 29, 2000, the international application designated the United States, and the international application was published by the World Intellectual Property Organization (WIPO) under the Patent Cooperation Treaty (PCT) Article 21(2) in the English language." *See, also* M.P.E.P. § 706.02(f)(1). Applicant submits that the foreign patent document (*i.e.,* FI 20011947) that Launiainen claims priority to does not meet all of these requirements. Thus, the effective date of the Launiainen reference under § 102(e) is Oct. 4, 2002 (*i.e.,* the U.S. filing date of the Launiainen reference). Therefore, Applicant submits that the Launiainen reference is not prior art under § 102(e), because the attached § 1.131 Declarations (executed by the inventors Andrei Terechko and Manish Garg) demonstrate that the filing date of the Launiainen reference does not predate the invention date of the claimed invention. Accordingly, Applicant requests that the § 102(e) rejection of claims 1-2, 8-9, 11-12, 14-17, 19-20 and 25-26 and the § 103(a) rejection of claim 10 be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of Philips Corporation at (408) 474-9063.

*Please direct all correspondence to:*

Corporate Patent Counsel
Philips Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

By: 

Name: Robert J. Crawford
Reg. No.: 32,122
(NXPS.208PA)

CUSTOMER NO. 24738

Attachments:
Two Declarations (§1.131) with Exhibit A.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | TERECHKO *et al.* | Examiner: | Cao, Chun |
| Serial No.: | 10/561,625 | Group Art Unit: | 2115 |
| Filed: | December 19, 2005 | Docket No.: | NL 021505 US |
| New Title: | ARRANGEMENT AND METHOD FOR CONTROLLING POWER MODES OF HARDWARE RESOURCES | | |

## INVENTOR DECLARATION (UNDER 37 C.F.R. §1.131)

I hereby state and declare that I, Andrei Terechko, am an inventor of the subject matter described and claimed and for which a U.S. Patent is sought on the invention entitled "Arrangement And Method For Controlling Power Modes Of Hardware Resources", having U.S. Patent Application Serial Number 10/561,625 (Docket No. NXPS.208PA), filed on December 19, 2005, which claims priority to U.S. provisional application number 60/430,884, filed on December 4, 2002.

I, Andrei Terechko, further state that:

1. The invention claimed in the above-referenced application was conceived of prior to October 4, 2002 and pursued with due diligence from prior to October 4, 2002 to the filing date of December 4, 2002. Attached to this Declaration are copies of an invention disclosure (labeled for this submission as Exhibit A), which indicate that the claimed invention was conceived of prior to October 4, 2002 (date having been redacted). In November of 2002, I conferred with an Attorney, Scott Stinebruner, who drafted the application that was filed as U.S. provisional application number 60/430,884 on December 4, 2002 (*i.e.*, constructive reduction to practice).

2. Using claim 1 as a representative claim, page 1 of Exhibit A evidences the invention in that it discusses controlling the power modes of resources of a processor using a power control instruction (*i.e.*, power_down operation). The same power_down operation can control the power modes of multiple resources. For example, the power_down operation specifies which registers can be used during a given cycle and the remaining registers can be

disabled during that cycle (*i.e.*, instructions are processed while the remaining registers are disabled in response to the power_down operation).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: July 09, 2008 Signature: _____

Andrei Terechko

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | TERECHKO *et al.* | Examiner: | Cao, Chun |
| Serial No.: | 10/561,625 | Group Art Unit: | 2115 |
| Filed: | December 19, 2005 | Docket No.: | NL 021505 US |
| New Title: | ARRANGEMENT AND METHOD FOR CONTROLLING POWER MODES OF HARDWARE RESOURCES | | |

## INVENTOR DECLARATION (UNDER 37 C.F.R. §1.131)

I hereby state and declare that I, Manish Garg, am an inventor of the subject matter described and claimed and for which a U.S. Patent is sought on the invention entitled "Arrangement And Method For Controlling Power Modes Of Hardware Resources", having U.S. Patent Application Serial Number 10/561,625 (Docket No. NXPS.208PA), filed on December 19, 2005, which claims priority to U.S. provisional application number 60/430,884, filed on December 4, 2002.

I, Manish Garg, further state that:

1. The invention claimed in the above-referenced application was conceived of prior to October 4, 2002 and pursued with due diligence from prior to October 4, 2002 to the filing date of December 4, 2002. Attached to this Declaration are copies of an invention disclosure (labeled for this submission as Exhibit A), which indicate that the claimed invention was conceived of prior to October 4, 2002 (date having been redacted). In November of 2002, I conferred with an Attorney, Scott Stinebruner, who drafted the application that was filed as U.S. provisional application number 60/430,884 on December 4, 2002 (*i.e.*, constructive reduction to practice).

2. Using claim 1 as a representative claim, page 1 of Exhibit A evidences the invention in that it discusses controlling the power modes of resources of a processor using a power control instruction (*i.e.*, power_down operation). The same power_down operation can control the power modes of multiple resources. For example, the power_down operation specifies which registers can be used during a given cycle and the remaining registers can be

disabled during that cycle (*i.e.*, instructions are processed while the remaining registers are disabled in response to the power_down operation).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: July 9th, 2008

Signature: _____
Manish Garg

Exhibit A

# *power_down* operation: a method to reduce power dissipation of microprocessors

**Inventors**
Andrei Terechko, Manish Garg

**Invention**
In the IC design of modern microprocessors power dissipation is one of the dominant constraints. This invention reveals a power_down operation for a VLIW, EPIC or superscalar processor that controls power modes for the processor resources (issue slots or function units, registers or register files, caches, etc.). This technique can especially help reduce energy consumption of wide-issue processors (e.g. TTI TriMedia, TI TMS320C6xxx, BOPS ManArray), where many parallel resources are not fully utilized throughout the program execution. In this case, the underutilized resources can be put into an energy saving mode by the power_down operation. In other cases, where strict power requirements are to be met, the compiler (or the programmer) can sacrifice performance for power, by scheduling operations not to all available resource and disabling the unused resources by the power_down operation. The power mode is changed either by the following power_down operation or by a processor exception/interrupt.

Consider the following assembly code in the TriMedia format. Let us assume the 128 registers of TriMedia are split in 8 banks 16 registers each. The bits of the immediate operand (0x1b is 11011) of the power_down operation in cycle 0 specify that only banks 1, 2, 4 and 5 should be activated. If the latency of power_down operation is 1 cycle, than in cycles 1, 2, 3, etc. banks 3, 6, 7, and 8 can be disabled and only registers from banks 1, 2, 4, and 5 can be used.

```
__tmMotEstTM32_DT_1:
  (* cycle 0 *)
        IF r1 ilesi(0) r12 -> r20,
        IF r1 power_down (0x1b),      (* disable banks 3, 6, 7, and 8 of the register file *)
        IF r1 ineqi(0) r35 -> r60,
        IF r1 ineqi(0) r34 -> r6,
        IF r1 ieqli(0) r35 -> r5;
  (* cycle 1 *)
        ...                           (* only registers from banks 1, 2 , 4, and 5 can be used *)
  (* cycle 2 *)
        ...                           (* only registers from banks 1, 2 , 4, and 5 can be used *)
  (* cycle 3 *)
        ...                           (* only registers from banks 1, 2 , 4, and 5 can be used *)
```

The same power_down operation can control power modes of issue slots, caches, writeback buses, etc.

Note that the power_down operation can be merged with the operations that access the processor control and status word (PCSW in TriMedia terms). The status word can be extended with the power enable bits that specify which resource is enabled at the moment. In this case, the power_down operation needs no dedicated opcode and can be executed in the form of the status word operations.

Most superscalar processor execute operations out-of-order. In this case, the compiler and hardware should limit reordering of the power_down operation such that it does not influence other speculated operations. In the superscalar processors this can be solved by assigning a side effect to the power_down operation, which limits its run-time speculation.

**Advantages**
In the TriMedia mediaprocessor with 128 registers, many applications require only 50% of the registers. Assuming that the register file consumes circa 20% of the total processor energy, our technique can reduce energy consumption of the CPU by over 10% if applied only to the register file.

Using the proposed technique the processor performance can be scaled up by, for example, adding registers or function units, but without increasing power dissipation on the code where the extra resources are not utilized. Moreover, for applications where the performance is not crucial the power_down operation can serve to sacrifice performance for lower power consumption.

**Disadvantages**
Instruction set architecture and compiler modifications are required.

**State-of-the-art**
*Clock gating* [1] is a common technique to eliminate switching activity in a circuit. Gating of the clock input is enabled by the processor control logic. This part of the control logic is active every cycle dissipating energy. Our technique avoids this switching activity in this part of the control logic. On top of that, clock gating can not address the problem of leakage power, while our technique can.

There exist *dual instruction set* (e.g. REAL DSPs) processors. One instruction set typically utilizes the processor fully, whereas the other restricted one uses only a part of the processor. Power consumption of the programs in the restricted instruction set is lower than in the full instruction set. In contrast to our technique, the dual instruction set allows for only two modes of processor utilization – full and restricted. The power_down operation technique is more flexible, enabling numerous energy consumption regimes for the processor.

Modern processors actively employ *voltage and frequency scaling* (Intel SpeedStep, Transmeta LongRun [2]). However, the scaling in these techniques is applied to the whole processor, while the power_down operation can select a processor resource and specify a particular power mode for it. Reduction of power consumption according to our method does not necessarily lead to performance losses. The scaling techniques are applicable only at longer periods of time (milliseconds), while our technique is more fine-grained and can control power in the range of nanoseconds.

Most processors have *WAIT* or *HALT* operations [3] to enter a sleep mode (StarCore, Intel x86). In this concept the processing is completely halted in contrast to the power_down method, in which the processing may continue on active resources.

*Multiple versions* of the code [4], which utilize different number of resources (e.g. registers), can be used to reduce energy consumption of the processor. This technique requires a run-time scheduler that selects a code version for execution, depending on the current power requirements. Evidently, multiple versions of code will require more program memory and execution of the scheduler, which all may result in a higher energy consumption than the saved power! The time granularity of this power control method is the function or thread, while our technique can control independent resources per scheduling unit (e.g. region, trace, or a decision tree of basic blocks) or even per basic block.

**References**

1. US5951689A1, "Microprocessor power control system", VLSI Technology.
2. http://www.transmeta.com/about/press/white_papers.html
3. US6343363, "Method of invoking a low power mode in a computer system using a halt instruction". National Semiconductor Corporation.
4. A. Azevedo, R. Cornea, et al., "Architectural and Compiler Strategies for Dynamic Power Management in the COPPER project", *Proceedings of the Innovative Architecture for Future Generation High-Performance Processors and Systems*, 18–19 January 2001 — Maui, Hawaii.